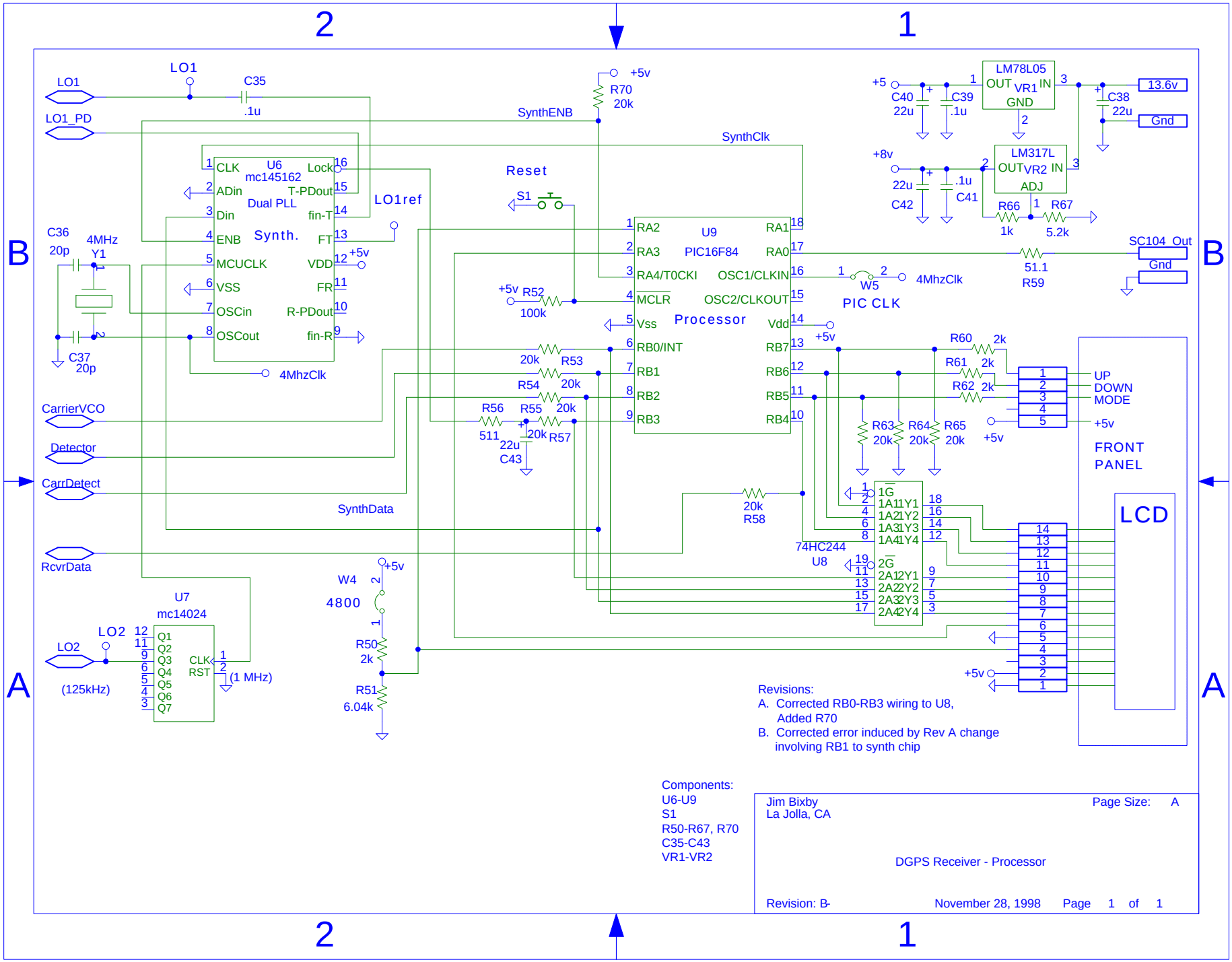
LO1
LO1_PD
C35
.1u
SynthENB
R70
20k
+5v
SynthClk
U6
mc145162
Dual PLL
Synth.
CLK
ADin
Din
ENB
MCUCLK
VSS
OSCin
OSCout
Lock
T-PDout
fin-T
FT
VDD
FR
R-PDout
fin-R
LO1ref
4MhzClk
C36
20p
4MHz
Y1
C37
20p
Reset
S1
U9
PIC16F84
Processor
RA2
RA3
RA4/T0CKI
MCLR
Vss
RB0/INT
RB1
RB2
RB3
RA1
RA0
OSC1/CLKIN
OSC2/CLKOUT
Vdd
RB7
RB6
RB5
RB4
R52
100k
R53
20k
R54
20k
R55
20k
R56
511
R57
20k
C43
22u
R58
20k
W5
4MhzClk
PIC CLK
R59
51.1
SC104_Out
Gnd
LM78L05
VR1
OUT
IN
GND
C40
22u
C39
.1u
C38
22u
13.6v
Gnd
LM317L
VR2
OUT
IN
ADJ
C42
22u
C41
.1u
R66
1k
R67
5.2k
R60
2k
R61
2k
R62
2k
R63
20k
R64
20k
R65
20k
UP
DOWN
MODE
FRONT
PANEL
LCD
74HC244
U8
1G
1A1
1A2
1A3
1A4
1Y1
1Y2
1Y3
1Y4
2G
2A1
2A2
2A3
2A4
2Y1
2Y2
2Y3
2Y4
CarrierVCO
Detector
CarrDetect
SynthData
RcvrData
U7
mc14024
LO2
(125kHz)
Q1
Q2
Q3
Q4
Q5
Q6
Q7
CLK
RST
(1 MHz)
W4
4800
R50
2k
R51
6.04k
Revisions:
A. Corrected RB0-RB3 wiring to U8,
Added R70
B. Corrected error induced by Rev A change
involving RB1 to synth chip
Components:
U6-U9
S1
R50-R67, R70
C35-C43
VR1-VR2
Jim Bixby
La Jolla, CA
Page Size: A
DGPS Receiver - Processor
Revision: B-
November 28, 1998
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